Confirmation No. 4536

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	VENEZIA *et al.*	Examiner:	Tsai, H.
Serial No.:	10/539,224	Group Art Unit:	2895
Filed:	June 16, 2005	Docket No.:	BE020043 US1 (NXPS.273PA)
Title:	METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE OBTAINED WITH SUCH A METHOD		

AMENDMENT TO APPEAL BRIEF

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P.O. Box 1450
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Customer No.
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Dear Sir:

This Amendment is submitted pursuant to 37 C.F.R. §41.37, in support of the Appeal Brief filed April 17, 2009 and in response to the Notification of Non-Compliant Appeal Brief (37 CFR 41.37) dated August 6, 2009.

If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

The Notification failed to explain the basis for the rejection other than checking box 4(a), which is derived from 37 CFR 41.37(c)(1)(v). On August 7, 2009, Examiner Sue A. Purvis indicated over the telephone that the brief was rejected because the summary did not include a description of dependent claims 3-9. After Appellant reviewed the file history for allegations of means plus function or step plus function limitations, Appellant attempted (on August 7, 2009) to contact Examiner Purvis to clarify the basis for the Notification of Non-Compliance, but was unsuccessful. Appellant submits that the summary meets all requirements of 37 CFR 41.37(c)(1)(v) because none of the dependent claims are alleged to include means plus function or step plus function limitations.

Appellant does not wish to have the instant Appeal Brief rejected by the Board (or other U.S.P.T.O. persons) for including material in the summary of limitations that is not

required by 37 CFR 41.37(c)(1)(v). In particular, the dependent claims do not contain means plus function or step plus function limitations. Accordingly, the following Examiner-required amendments include a statement that the amended summary was required by U.S.P.T.O. personnel.

Appellant presents the amendment in the form of a paper providing a summary of the claimed subject matter per M.P.E.P. 1205.03: "...an entire new brief need not, and should not, be filed. Rather, a paper providing a summary of the claimed subject matter as required by 37 CFR 41.37(c)(1)(v) will suffice."

V. Summary of Claimed Subject Matter

This summary includes a summary of dependent claims 3-9, which Examiner Sue A. Purvis indicated was required. The inclusion of these claims is not a representation that the claims include means plus function or step plus function limitations.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a method of manufacturing a semiconductor device (*see, e.g.*, device 10 shown in Figs. 1-6) with a semiconductor body of a semiconductor material (*see, e.g.*, body 1 shown in Figs. 1-6, and page 5:3-5), the semiconductor device including a field effect transistor having a source region and a drain region (*see, e.g.*, source and drain regions 2 and 3 shown in Fig. 3, and page 5:20-24) at a surface of the semiconductor body, and having a gate region (*see, e.g.*, gate 4 shown in Fig. 3) between the source region and the drain region, the gate region including a semiconductor region of a further semiconductor material (*see, e.g.*, polycrystalline region 4A shown in Fig. 3) that is separated from the surface of the semiconductor body by a gate dielectric (*see, e.g.*, gate oxide 5 shown in Fig. 3), the method comprising: forming the gate dielectric on the surface of the semiconductor body (*see, e.g.*, page 5:13-19); forming the semiconductor region on the gate dielectric (*see, e.g.*, page 5:13-19); depositing a sacrificial region (*see, e.g.*, sacrificial region 4B shown in Fig. 3, and page 5:13-19) on top of the semiconductor region; after depositing the sacrificial region, forming spacers (*see, e.g.*, spacers 6 shown in Fig. 3, and page 5:24-30) adjacent to the gate region for forming the source and drain regions; forming the source and drain regions on the surface of the semiconductor body (*see, e.g.*, Fig. 3, and page 5:30-33); after forming the source and drain regions, selectively etching the sacrificial region with respect to the semiconductor region (*see, e.g.*, Fig. 4, and page 6:1-6); depositing a metal layer (*see, e.g.*, metal layer 7 shown in Fig. 4, and page 6:6-10) on the source region, the drain region, and the gate region; forming a compound (*see, e.g.*, region 8A shown Fig. 5, and page 6:11-20), that includes at least a portion of the source and drain regions, of the metal layer and the semiconductor material; and forming a compound (*see, e.g.*, region 8B shown Fig. 5, and page 6:11-20), that

includes at least a substantial portion of the further semiconductor material, of the metal layer and the further semiconductor material.

Commensurate with dependent claim 3, a method as claimed in claim 1, characterized in that the further semiconductor region (*see, e.g.*, polycrystalline region 4A shown in Fig. 3) is completely consumed during the formation of the compound of the metal layer and the further semiconductor material (*see, e.g.*, region 8B shown Fig. 5, and page 6:11-20).

Commensurate with dependent claim 4, a method as claimed in claim 1, characterized in that the formation of the compounds between the metal and the semiconductor material and the metal and the further semiconductor material is carried out in two separate heating steps (*see, e.g.*, Fig 5, page 6:11-20), the first heating step resulting in an intermediate compound with a low content of the semiconductor material or of the further semiconductor material (*see, e.g.*, page 6:11-20 and page 6:31-7:4) and in the second heating step the intermediate compound being converted to the compound having a higher content of the semiconductor material or of the further semiconductor material (*see, e.g.*, page 6:11-20 and page 6:31-7:4).

Commensurate with dependent claim 5, a method as claimed in claim 4, characterized in that between the two heating steps, a part of the metal layer which has not reacted to form the intermediate compound is removed by etching (*see, e.g.*, page 6:31-7:4).

Commensurate with dependent claim 6, a method as claimed in claim 4, characterized in that between the two heating steps, a layer of the further semiconductor material is deposited on the surface of the semiconductor body (*see, e.g.*, Figs. 7 and 8, and page 6:31-7:4).

Commensurate with dependent claim 7, a method as claimed in claim 6, characterized in that after the second heating step, a part of the layer of the further semiconductor material which has not reacted to form the compound is removed by etching (*see, e.g.*, page 7:4-6).

Commensurate with dependent claim 8, a method as claimed in claim 1, characterized in that after the formation of the compounds of the metal and the semiconductor material and of the metal and the further semiconductor material, the spacers are removed (*see, e.g.*, Fig. 6, and page 6:21-24).

Commensurate with dependent claim 9, a method as claimed in claim 4, characterized in that for the semiconductor material as well as for the further semiconductor material silicon is chosen (*see, e.g.*, page 5:8-11), and for the intermediate compound and for the compound of the metal and the semiconductor material and the further semiconductor material a metal silicide is chosen (*see, e.g.*, page 6:33-7:2).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Authority to charge the undersigned's deposit account was provided on the first page of this amendment.

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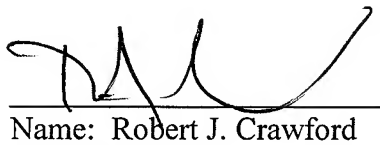
By: 

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